

NCE 30V Half Bridge Dual N-Channel Enhancement Mode Power MOSFET

Description

The NCEB301G is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. It includes two specialized MOSFETs in a dual Power DFN5x6 package. The Q1 "High Side" MOSFET is designed to minimize switching losses. The Q2 "Low Side" MOSFET uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge.

Application

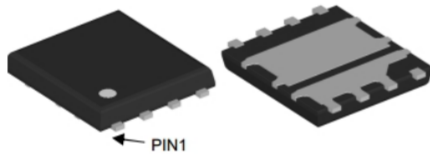
- Compact DC/DC converter applications
- Synchronous buck converters

Q1 "High Side" MOSFET

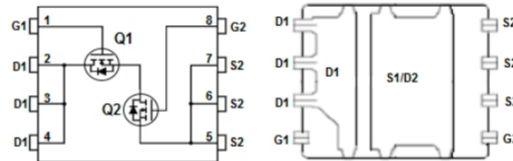
- $V_{DS} = 30\text{ V}, I_D = 20\text{ A}$
- $R_{DS(ON)} < 7.2\text{ m}\Omega @ V_{GS}=10\text{ V}$ (typical: 6.1 m Ω)
- $R_{DS(ON)} < 12.5\text{ m}\Omega @ V_{GS}=4.5\text{ V}$ (typical: 9.6 m Ω)

Q2 "Low Side" MOSFET

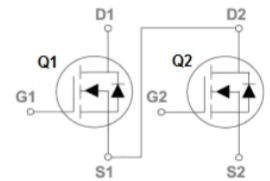
- $V_{DS} = 30\text{ V}, I_D = 35\text{ A}$
- $R_{DS(ON)} < 4.1\text{ m}\Omega @ V_{GS}=10\text{ V}$ (typical: 3.5 m Ω)
- $R_{DS(ON)} < 7.8\text{ m}\Omega @ V_{GS}=4.5\text{ V}$ (typical: 5.9 m Ω)
- Excellent gate charge x $R_{DS(on)}$ (FOM)
- Very low on-resistance $R_{DS(on)}$
- 150°C operating temperature
- Pb-free lead plating
- 100% UIS tested



Top View Bottom View
Dual PDFN5×6-8L



Pin Assignment



Schematic Diagram

Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
B301G	NCEB301G	PDFN5×6-8L	Ø330mm	12mm	5000units

Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Q1	Q2	Unit
Drain-Source Voltage	V_{DS}	30	30	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current	I_D	20	35	A
Continuous Drain Current ($T_c=100^\circ\text{C}$)	$I_{D(100^\circ\text{C})}$	20	35	A
Pulsed Drain Current	I_{DM}	80	140	A
Maximum Power Dissipation	P_D	20	40	W
Single pulse avalanche energy ^(Note 1)	E_{AS}	100	207	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150		$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Case(Q1)	$R_{\theta JC}$	6.3	$^{\circ}C/W$
Thermal Resistance, Junction-to-Case(Q2)	$R_{\theta JC}$	3.1	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient (Note 2)(Q1)	$R_{\theta JA}$	50	$^{\circ}C/W$
Thermal Resistance, Junction-to-Ambient (Note 2)(Q2)	$R_{\theta JA}$	50	$^{\circ}C/W$

Q1 N-Channel Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.6	2.3	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$	-	6.1	7.2	m Ω
		$V_{GS}=4.5V, I_D=10A$	-	9.6	12.5	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=13A$	-	32	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $F=1.0MHz$	-	960	-	pF
Output Capacitance	C_{oss}		-	157	-	pF
Reverse Transfer Capacitance	C_{rss}		-	140	-	pF
Switching Characteristics (Note 3)						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=15V, R_L=0.75\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	7	-	nS
Turn-on Rise Time	t_r		-	5	-	nS
Turn-off Delay Time	$t_{d(off)}$		-	26	-	nS
Turn-off Fall Time	t_f		-	7	-	nS
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=15A,$ $V_{GS}=10V$	-	24	-	nC
Gate-Source Charge	Q_{gs}		-	3	-	nC
Gate-Drain Charge	Q_{gd}		-	6	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
Diode Forward Current	I_S		-	-	20	A
Reverse Recovery Time	t_{rr}	$T_J = 25^{\circ}C, I_F = 20A$ $di/dt = 100A/\mu s$	-	11	-	nS
Reverse Recovery Charge	Q_{rr}		-	15	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Q2 N-Channel Electrical Characteristics ($T_C=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	30	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=30V, V_{GS}=0V$	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA

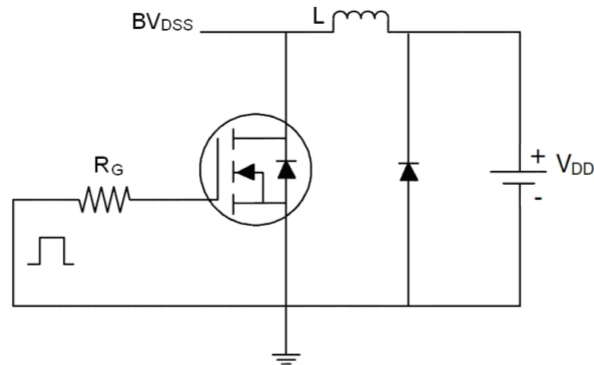
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.6	2.2	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=12A$	-	3.5	4.1	m Ω
		$V_{GS}=4.5V, I_D=10A$	-	5.9	7.8	m Ω
Forward Transconductance	g_{FS}	$V_{DS}=10V, I_D=20A$	-	30	-	S
Dynamic Characteristics						
Input Capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $F=1.0MHz$	-	1784	-	pF
Output Capacitance	C_{oss}		-	266	-	pF
Reverse Transfer Capacitance	C_{rss}		-	212	-	pF
Switching Characteristics <small>(Note 3)</small>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=15V, R_L=1.5\Omega$ $V_{GS}=10V, R_G=6\Omega$	-	7	-	nS
Turn-on Rise Time	t_r		-	6	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	30	-	nS
Turn-Off Fall Time	t_f		-	8	-	nS
Total Gate Charge	Q_g	$V_{DS}=15V, I_D=20A$ $V_{GS}=10V$	-	38.4	-	nC
Gate-Source Charge	Q_{gs}		-	5.8	-	nC
Gate-Drain Charge	Q_{gd}		-	7.9	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=12A$	-	-	1.2	V
Diode Forward Current	I_S		-	-	35	A
Reverse Recovery Time	t_{rr}	$T_J = 25^\circ C, I_F = 20A$ $di/dt = 100A/\mu s$	-	47	-	nS
Reverse Recovery Charge	Q_{rr}		-	47	-	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

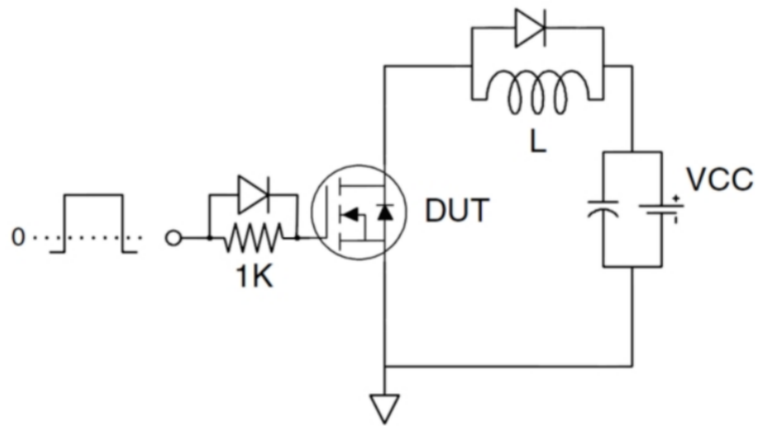
1. EAS condition : $T_J=25^\circ C, V_{DD}=25V, V_G=10V, L=0.5mH, R_g=25\Omega$.
2. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$. The maximum allowed junction temperature of $150^\circ C$. The value in any given application depends on the user's specific board design, and the maximum temperature of $150^\circ C$ may be used if the PCB allows it.
3. Guaranteed by design, not subject to production.
4. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heat sink, assuming a maximum junction temperature of $T_{J(MAX)}=150^\circ C$. The SOA curve provides a single pulse rating.

Test Circuit

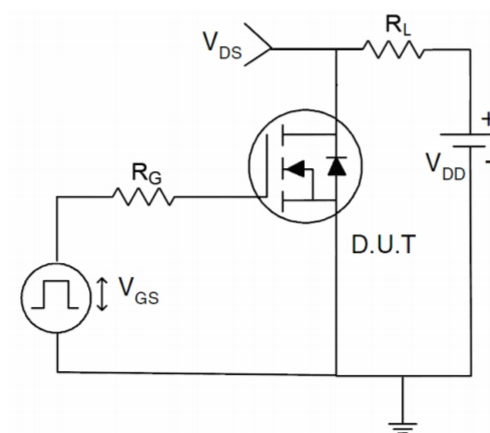
1) E_{AS} Test Circuit



2) Gate Charge Test Circuit



3) Switch Time Test Circuit



Q1 N-Channel Typical Electrical and Thermal Characteristics (Curves)

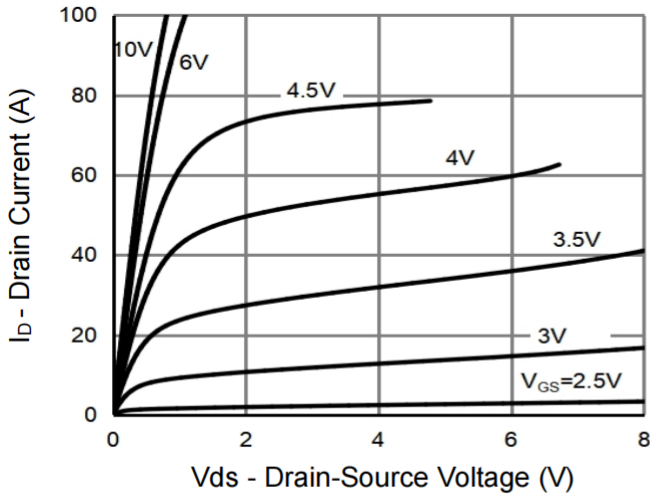


Figure 1 Output Characteristics

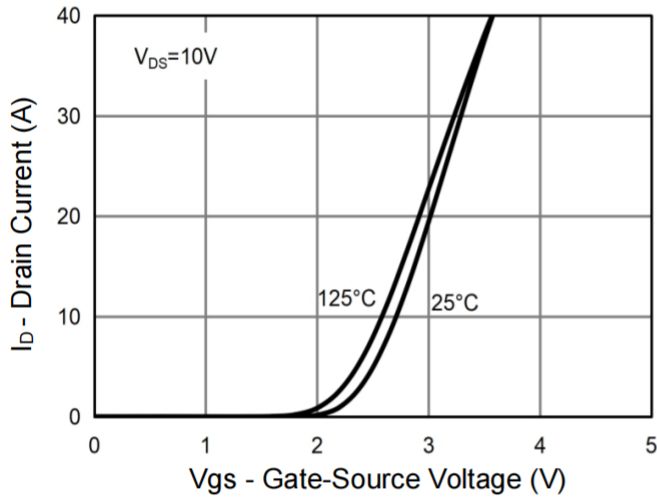


Figure 2 Transfer Characteristics

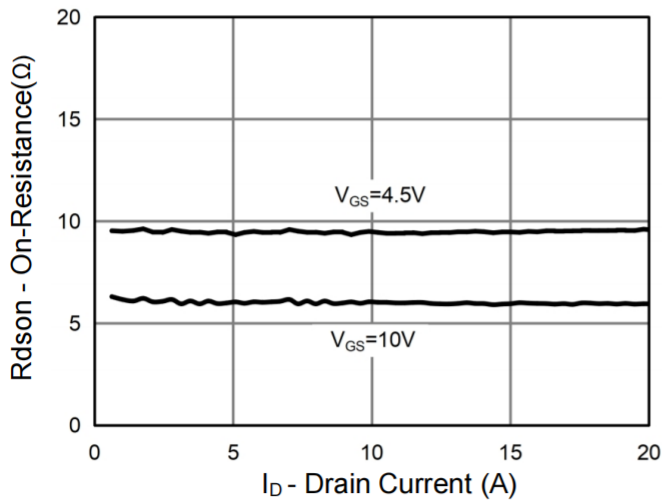


Figure 3 $R_{DS(on)}$ vs Drain Current

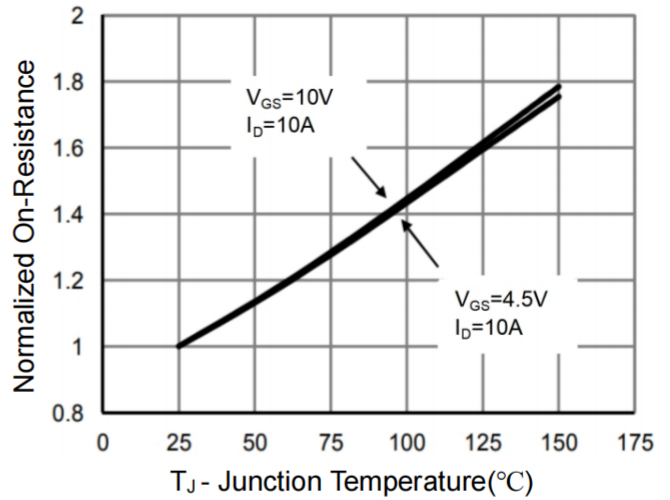


Figure 4 $R_{DS(on)}$ vs Junction Temperature

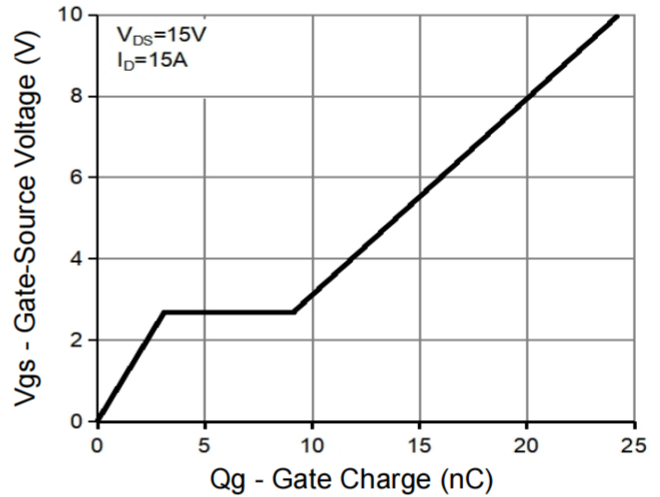


Figure 5 Gate Charge

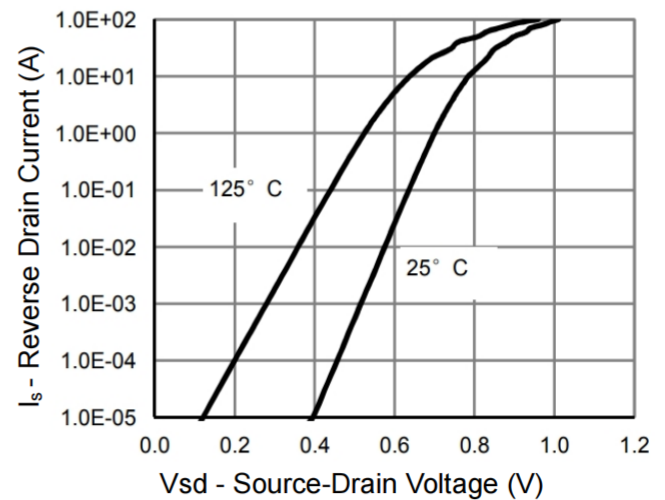


Figure 6 Source-Drain Diode Forward

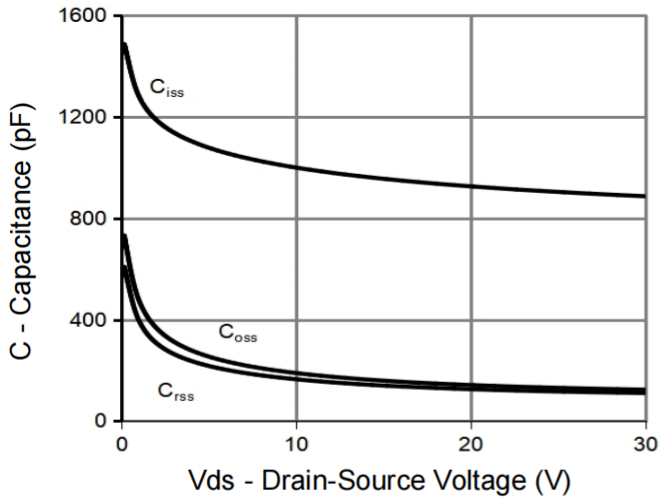


Figure 7 Capacitance vs Vds

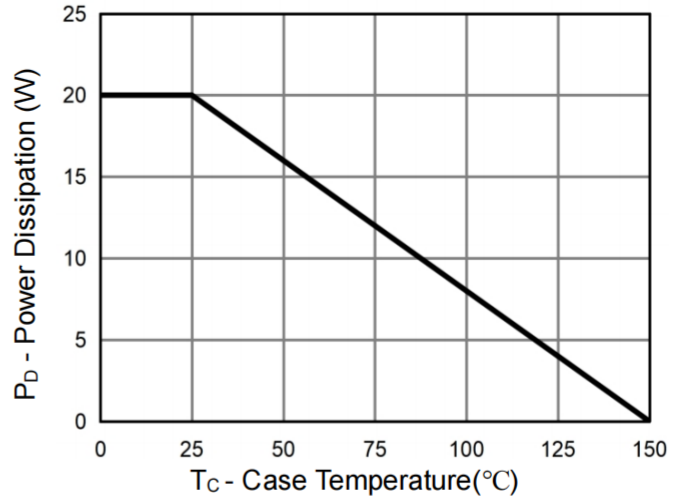


Figure 9 Power De-rating

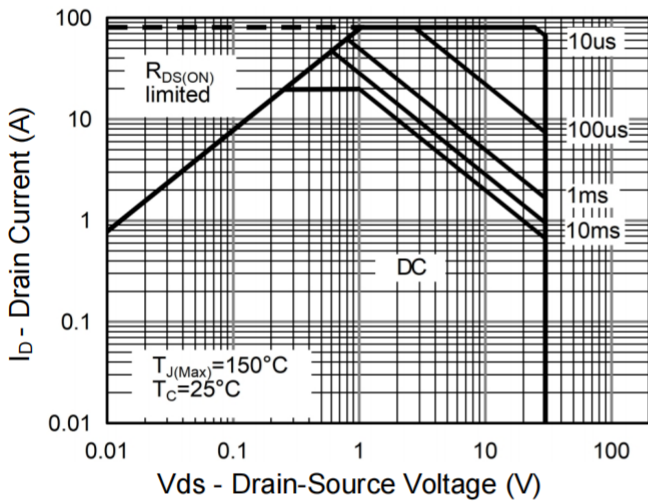


Figure 8 Safe Operation Area (Note 4)

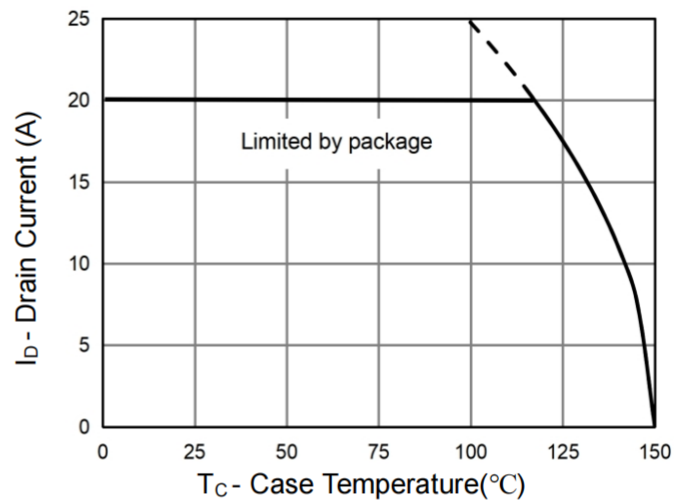


Figure 10 Drain Current De-rati

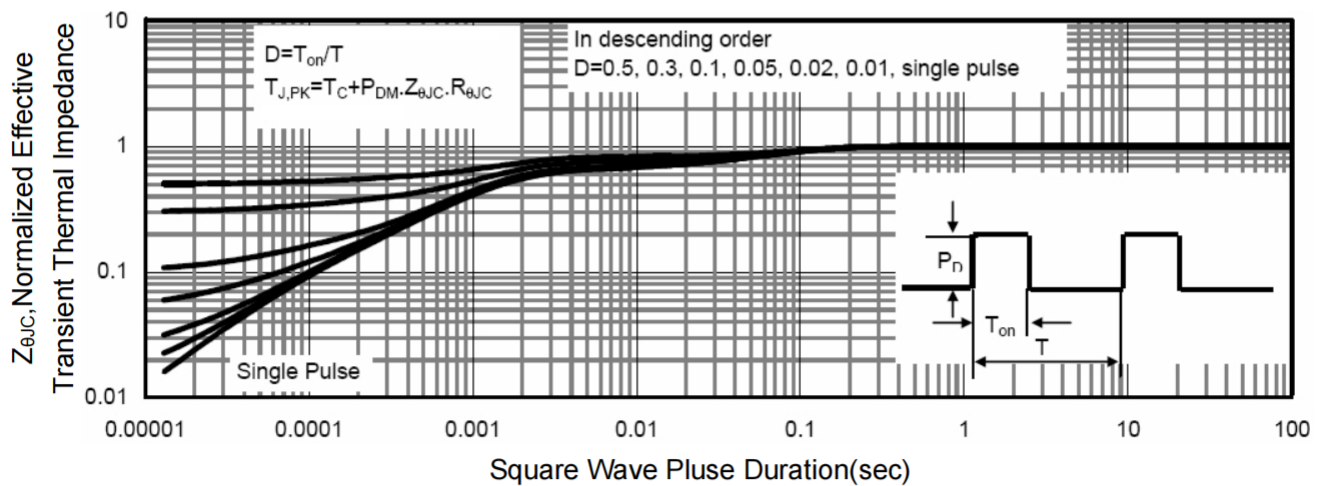


Figure 11 Normalized Maximum Transient Thermal Impedance

Q2 N-Channel Typical Electrical and Thermal Characteristics (Curves)

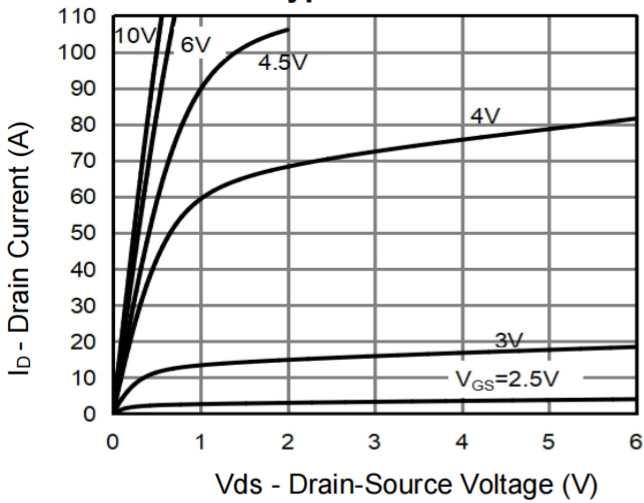


Figure 1 Output Characteristics

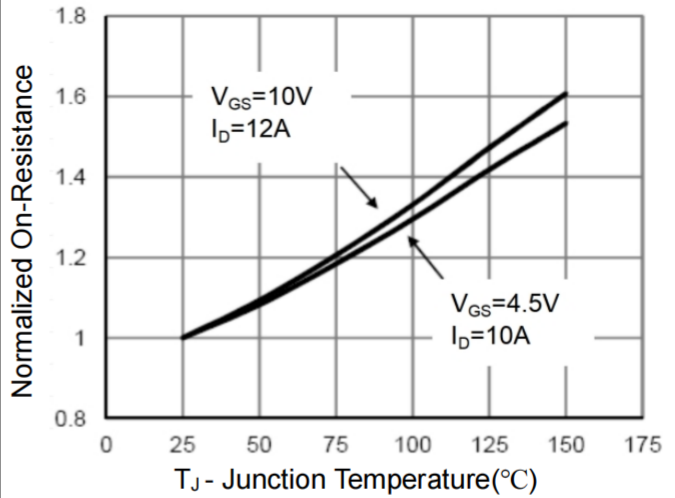


Figure 4 $R_{DS(on)}$ vs Junction Temperature

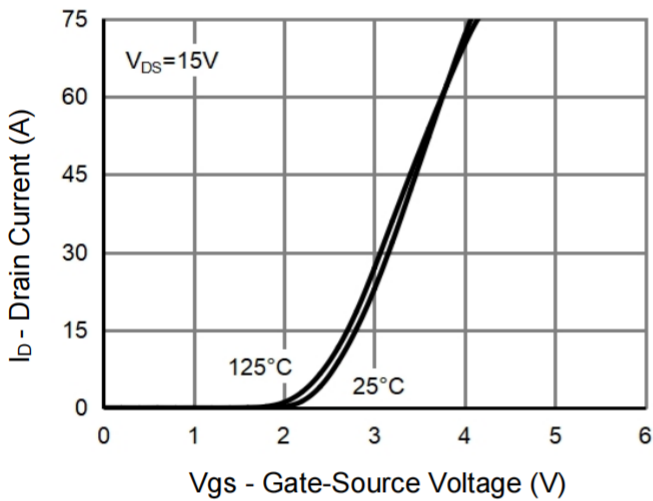


Figure 2 Transfer Characteristics

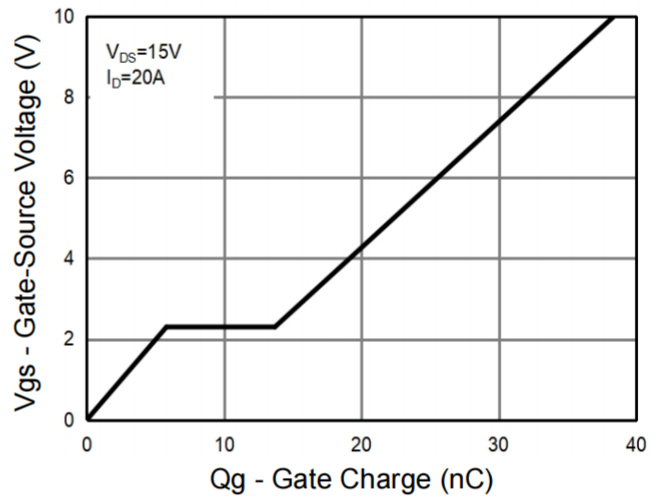


Figure 5 Gate Charge

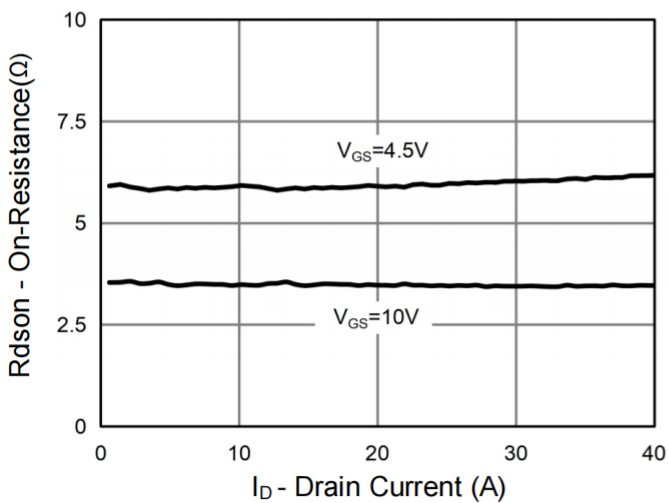


Figure 3 $R_{DS(on)}$ vs Drain Current

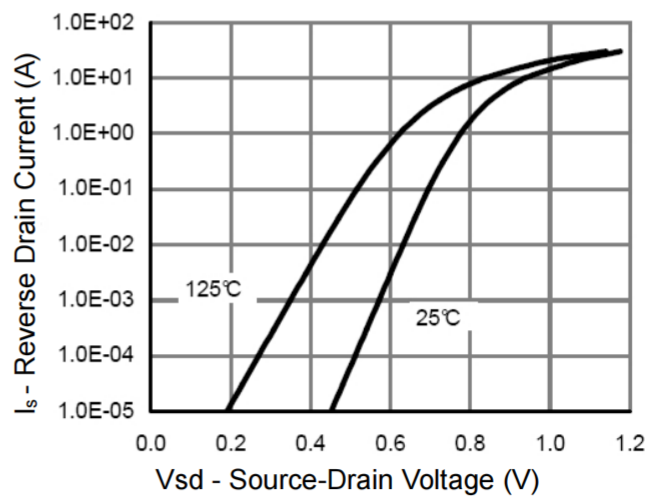


Figure 6 Source-Drain Diode Forward

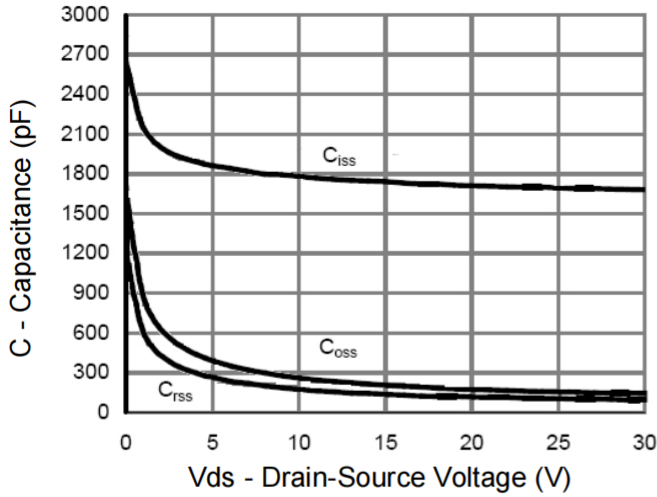


Figure 7 Capacitance vs Vds

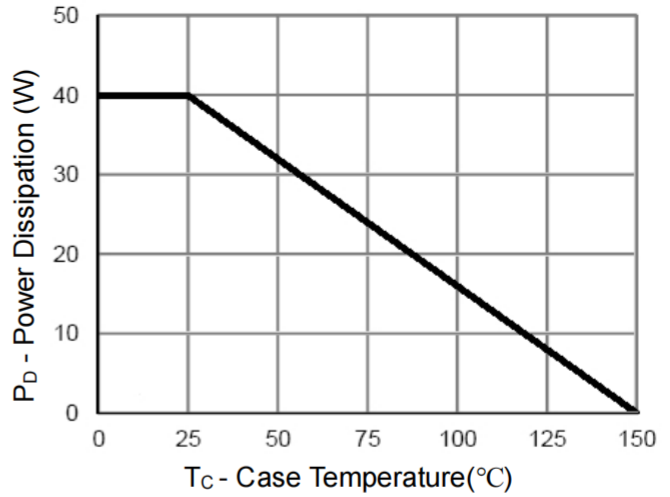


Figure 9 Power De-rating

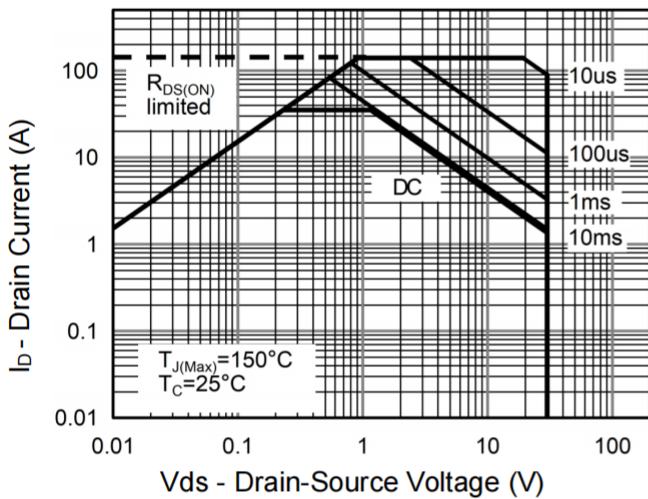


Figure 8 Safe Operation Area (Note 4)

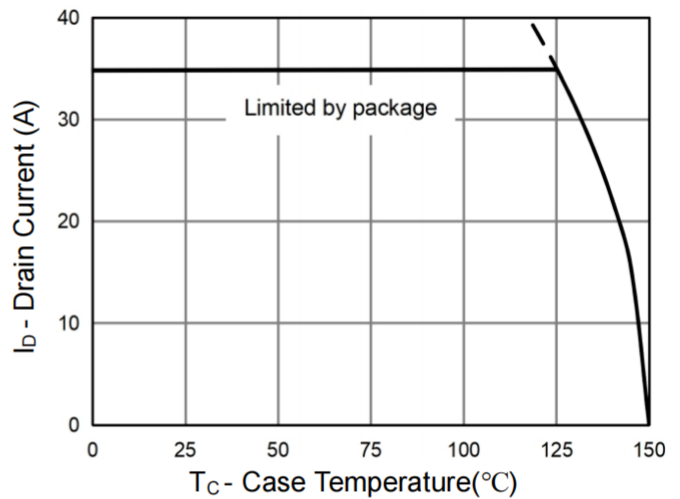


Figure 10 Drain Current De-rating

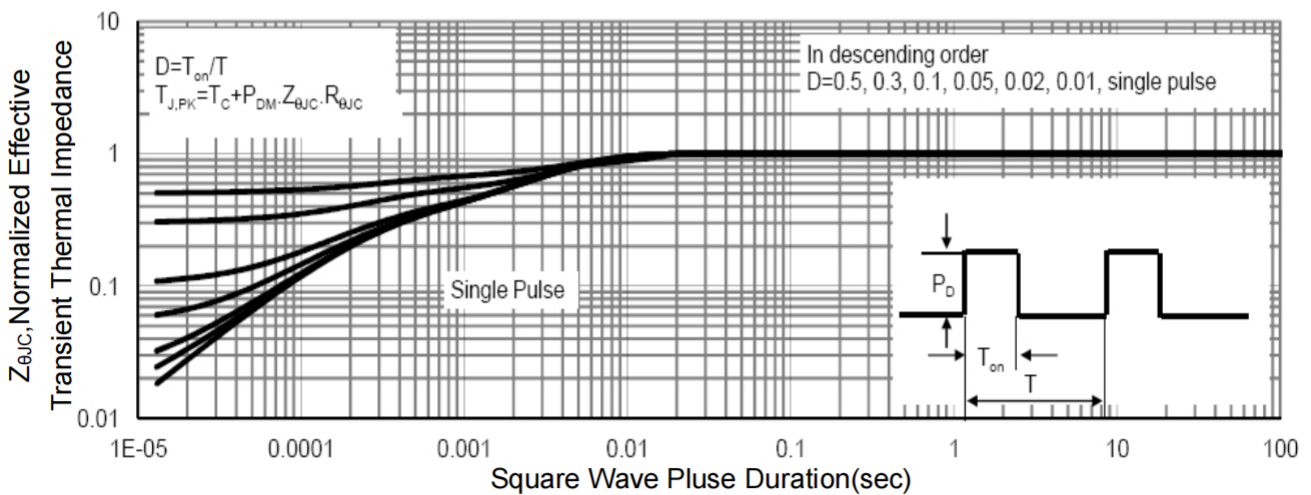
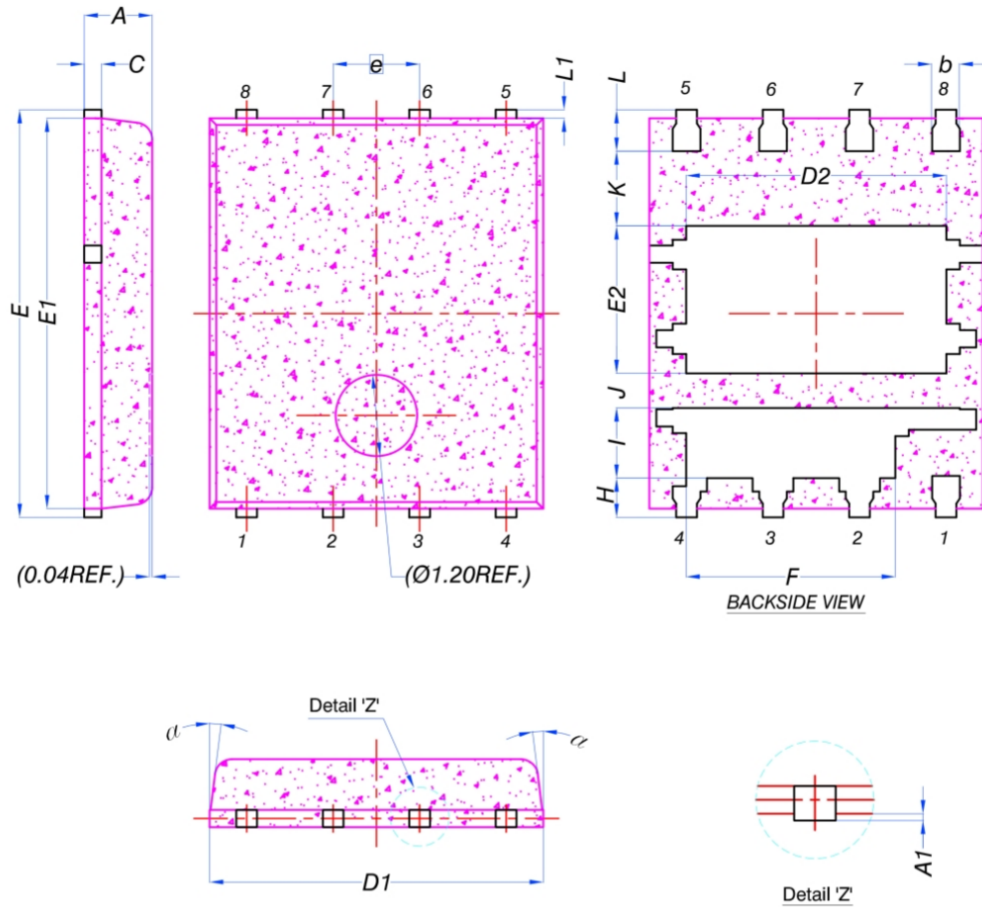


Figure 11 Normalized Maximum Transient Thermal Impedance

PDFN5×6-8L(G) Package Information



**Land Pattern
(Only for Reference)**

DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	---	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	2.02	2.17	2.32
e	1.27 BSC		
F	2.87	3.07	3.22
H	0.48	0.58	0.68
I	0.94	1.04	1.14
J	0.40	0.50	0.60
K	0.50	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°

Land pattern diagram showing dimensions for the solder mask and pad layout. Dimensions include 0.71, 3.96, 1.27, 0.61, 2.34, 1.29, 2.22, 0.00, 1.43, 1.95, 2.47, 3.05, 0.58, 2.92, 1.20, and 0.00.

Revision History

Revision	Date	Subjects
V2.0	2026.3	Update the parameters and curves.

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