JWP79336DM67

High-Performance All-in-one IPM For Motor Control

Preliminary Specifications Subject to Change without Notice

DESCRIPTION

JWP79336DM67 is a high-voltage integrated IPM for 3-phase motor drive applications. It integrates a control core, high-voltage MOSFETs, a three-channel pre-driver, and a 5V LDO, helping reduce external components and simplify system design.

FEATURES

- Integrated 32-bit Control Core, up to 108MHz
- Integrated Flash/SRAM Resources for Motor-Control Algorithms
- Integrated ADC/OPA/ACMP/DAC and Timer Peripherals for Motor Control
- Integrated High-voltage MOSFET Stage
- Integrated 3-phase Pre-driver with Built-in Dead-time and Delay Matching
- Integrated 5V LDO
- Pre-driver Protection Support: UVLO, OCP, and OTP
- 5V LDO Output Capability up to 100mA (with Proper Thermal Design)
- Operating Ambient Temperature Range: -40C to 125C
- Available in SSOPA54-38 Package

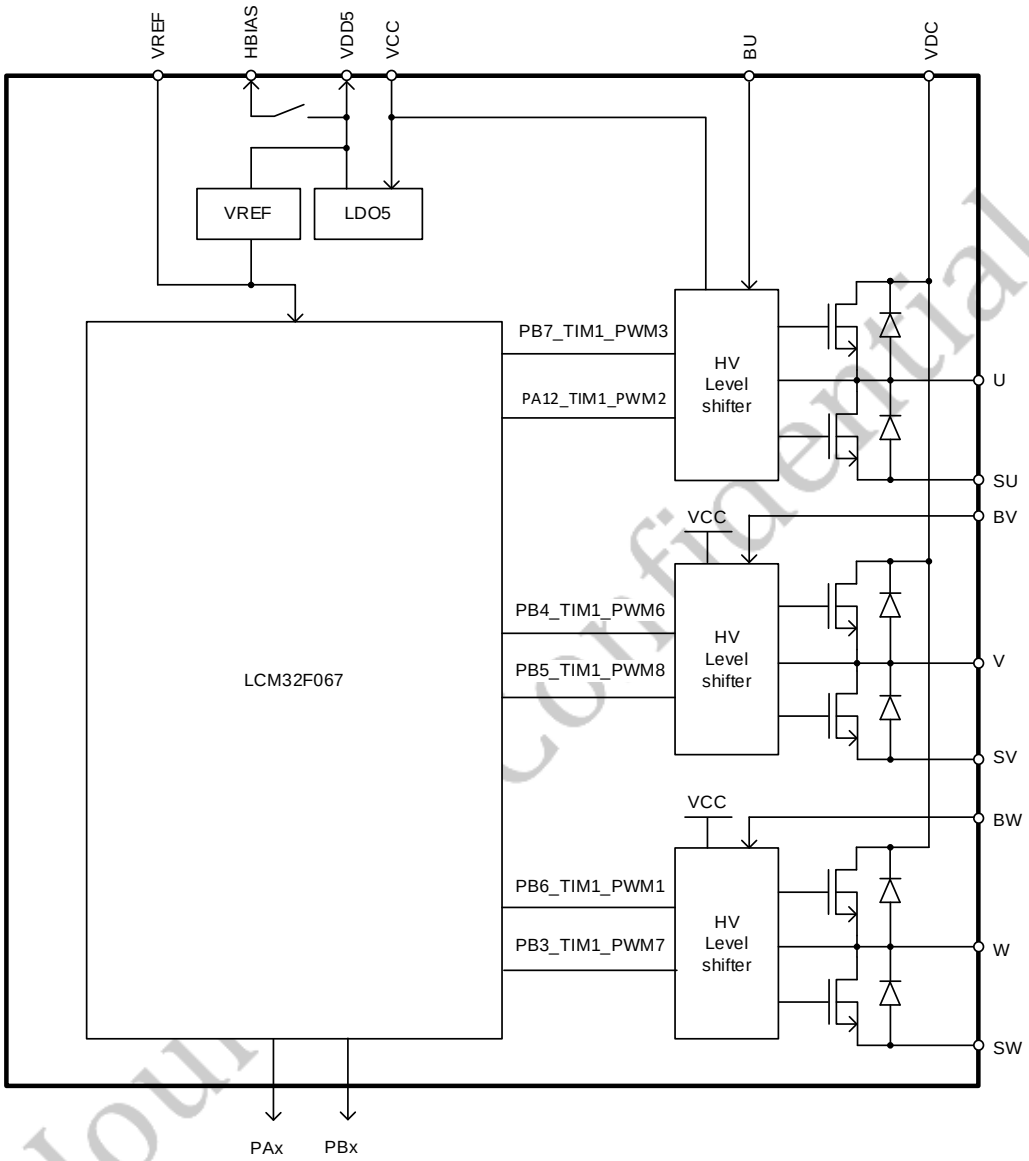
APPLICATIONS

- Air-conditioner Fan Motors
- Air Purifier Motors
- Water Pumps
- Washing Machine and Small Home Appliance Motors

Preliminary Specifications Subject to Change without Notice

CONTENTS

BLOCK DIAGRAM



INTERNAL SIGNAL CONNECTIONS

MCU SIGNAL	MCU FUNCTION	PRE-DRIVER FUNCTION
PB7	TIM1_PWM3_PWM output	HIN3
PA12	TIM1_PWM2_PWM output	LIN3
PB4	TIM1_PWM6_PWM output	HIN2
PB5	TIM1_PWM8_PWM output	LIN2
PB6	TIM1_PWM1_PWM output	HIN1
PB3	TIM1_PWM7_PWM output	LIN1

TYPICAL APPLICATION

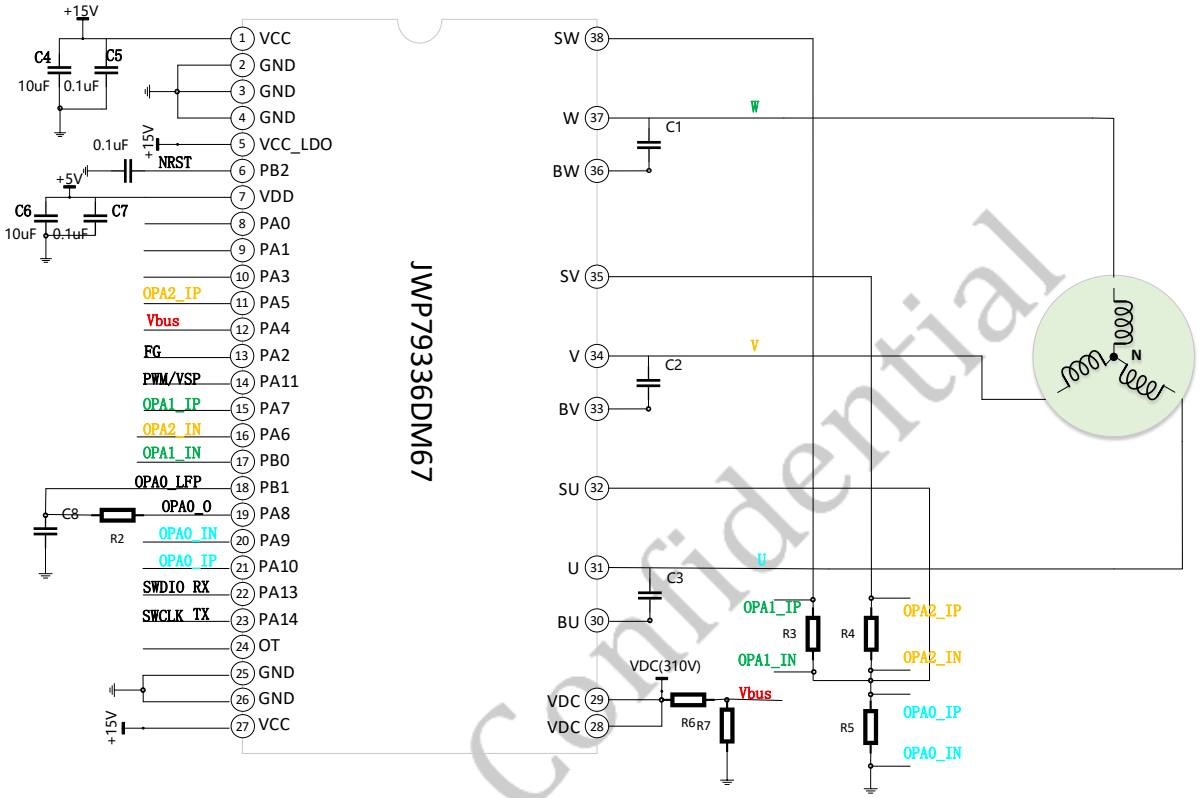


Figure 1. Sensorless Dual-Resistor Differential Sampling FOC Mode

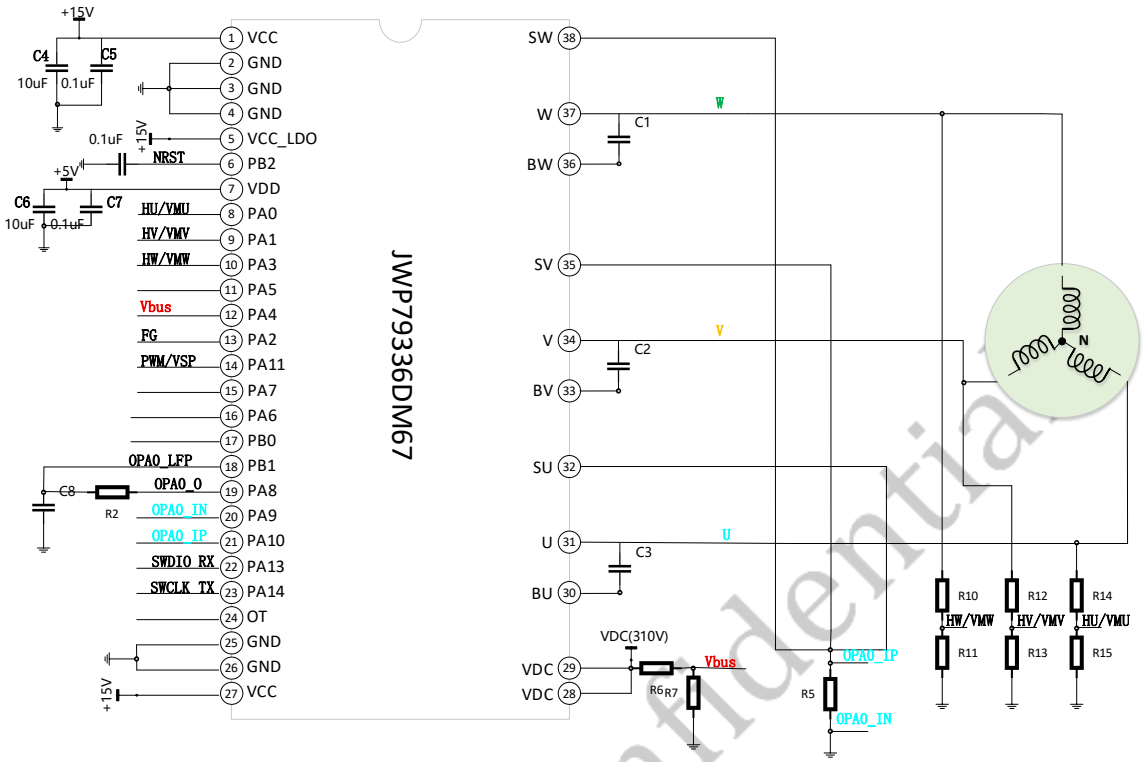


Figure 2. Single-Shunt Sensorless BLDC Drive Mode

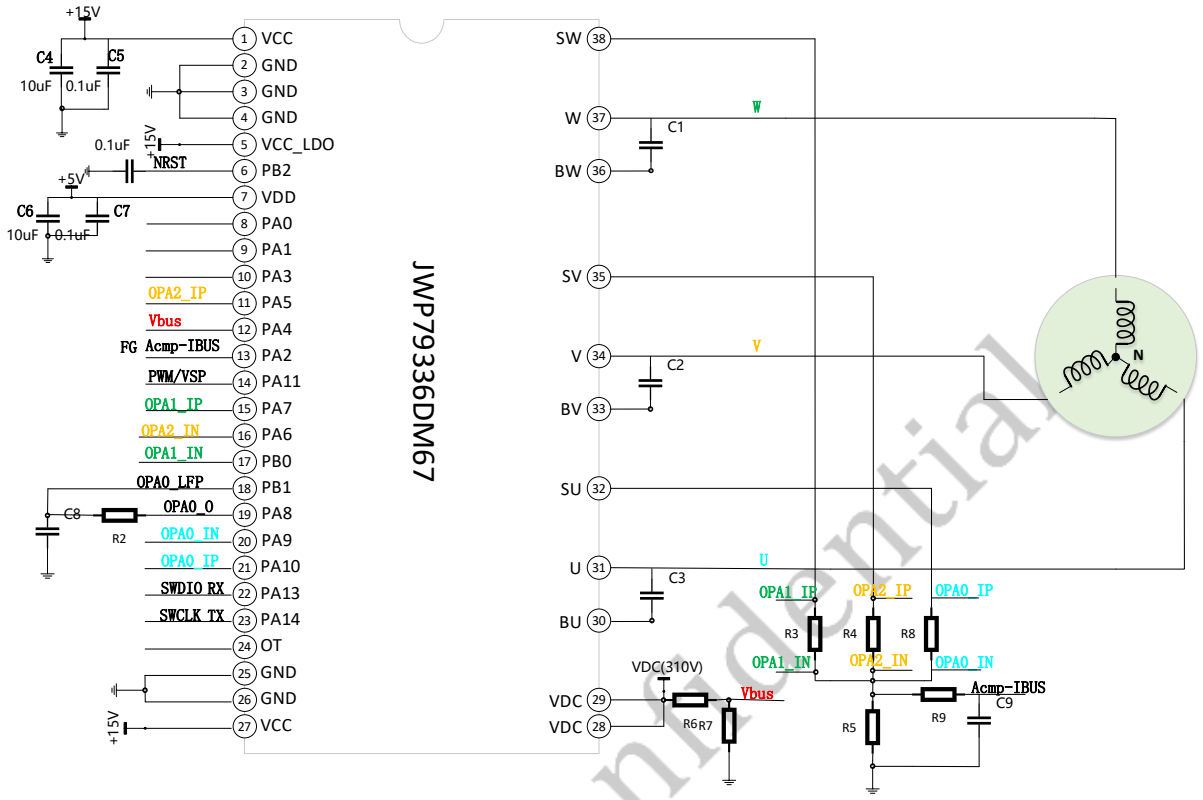


Figure 3. Sensorless Triple-Resistor Differential Sampling FOC Mode

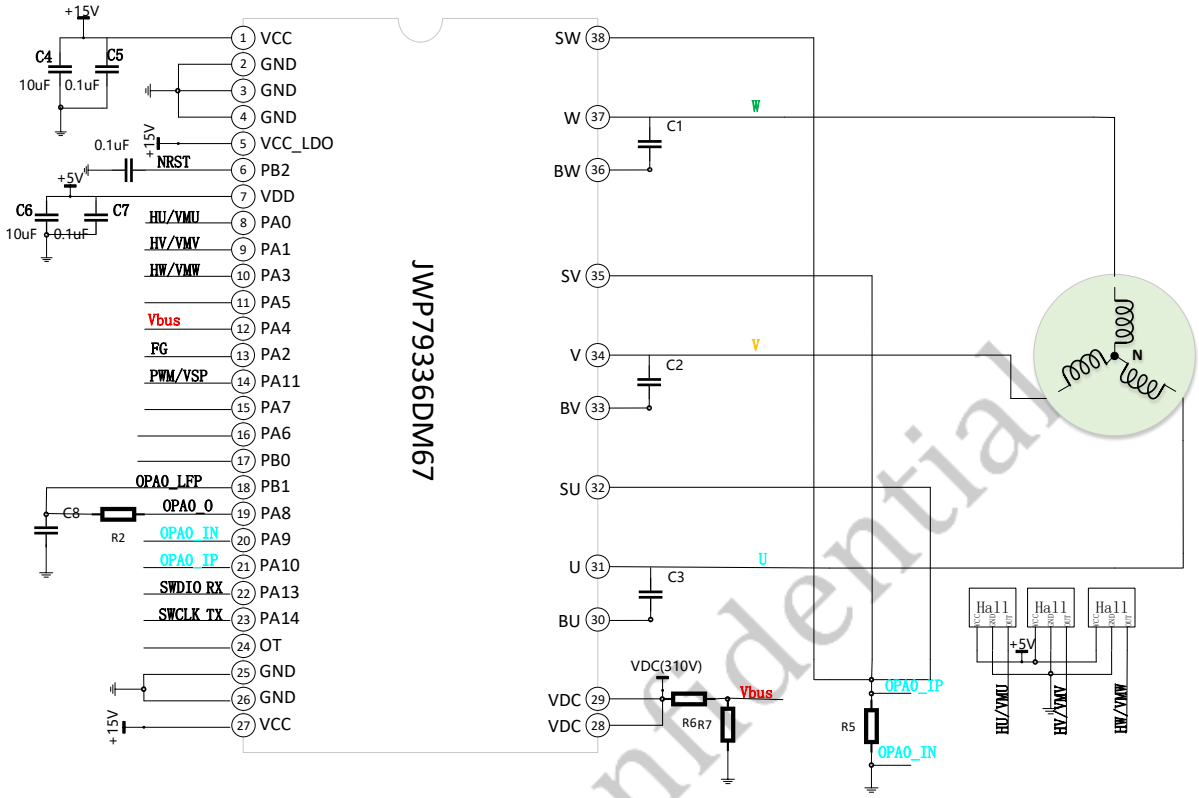


Figure 4. Sensored Single-Resistor Sampling FOC Mode

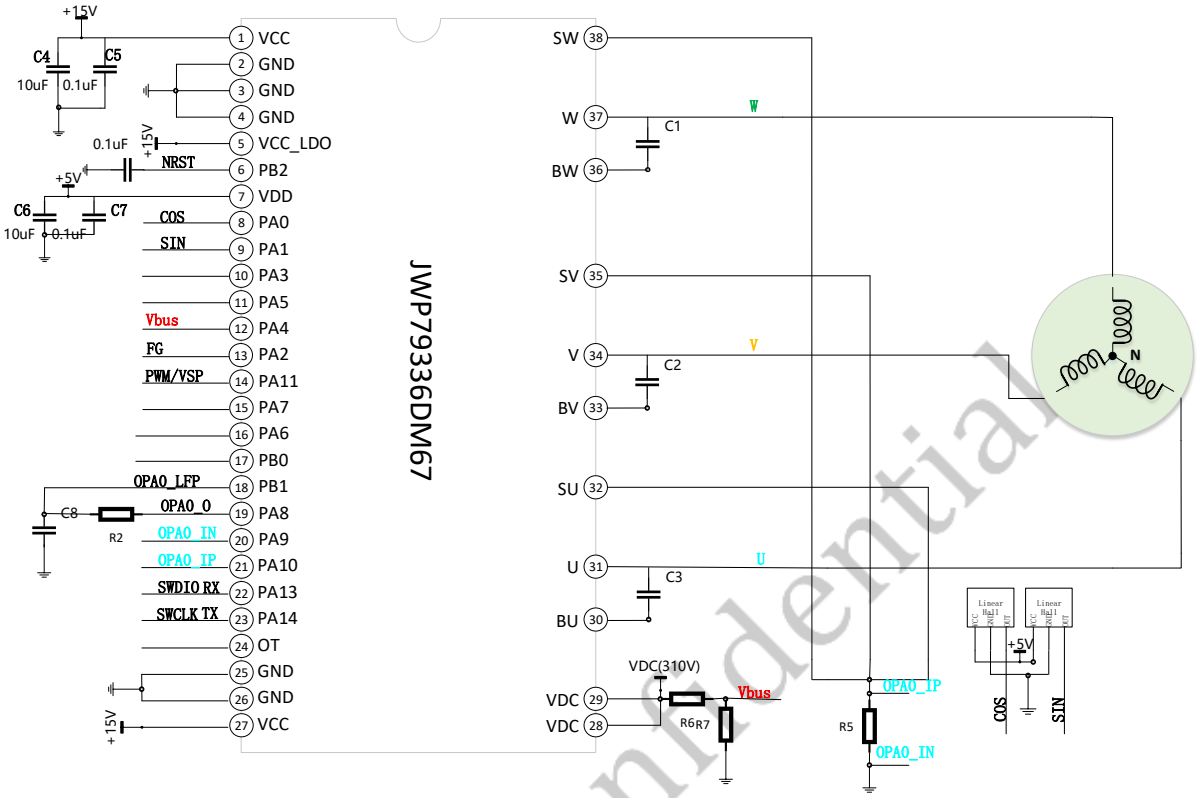


Figure 5. Linear Hall Single-Resistor Sampling FOC Mode

ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]	SHIPPING METHOD	MOQ (pcs/reel)
JWP79336DM67SSOWA#TR	SSOPA54-38	P79336DM67 YW□□□□□	Green	Tape & Reel	5000

Notes:

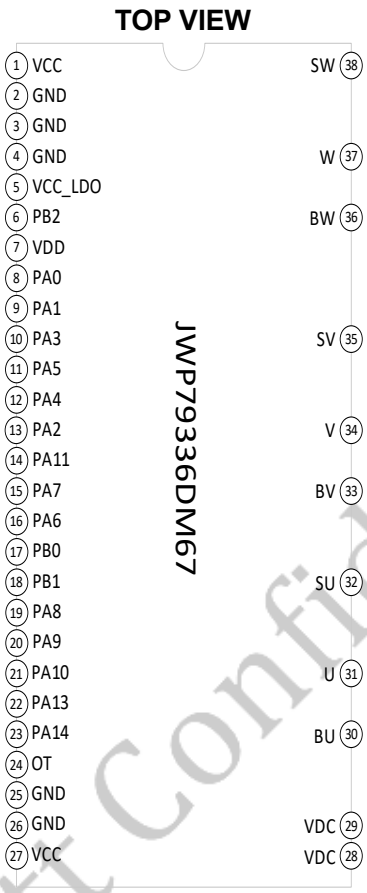
1) JW□□□□#TR
- Tape and Reel
- Package Code
- Part No.

2) Line1: JW □□□□
- Product code
- JoulWatt LOGO

Line2: YW □□□□□
- Lot number
- Week code
- Year code

3) All JoulWatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

PIN CONFIGURATION



PIN DESCRIPTION

PIN	NAME	DESCRIPTION
1	VCC	Power supply input
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	VCC_LDO	5V LDO Input
6	PB2	nRST
7	VDD	5V LDO Output
8	PA0	TIM2_CH1 / ADCIN[0] / ACMP0_P4
9	PA1	TIM2_CH2 / ADCIN[1] / ACMP0_P5
10	PA3	TIM2_CH3 / ADCIN[3] / ACMP0_P6
11	PA5	TIM15_CH1 / TIM16_CH2 / ADCIN[4] / ADCIN[5] / OPA2_P0
12	PA4	ADCIN[4]/ACMP1_P1/ ACMP1_out

13	PA2	TIM15_CH2
14	PA11	TIM15_CH1 / ADCIN[14]
15	PA7	TIM17_CH1 / ADCIN[7] / OPA1_P0 / ADCIN[12]
16	PA6	TIM16_CH1 / ADCIN[6] /OPA2_N1
17	PB0	ADCIN[4] / ADCIN[8] / OPA1_N0
18	PB1	ADCIN[2]
19	PA8	ADCIN[10] / OPA0_O
20	PA9	OPA0_N0
21	PA10	OPA0_P0
22	PA13	USART1_RX / SWDIO /DACOUT_BUF
23	PA14	USART1_TX / SWCLK
24	OT	Temperature Sensor Output
25	GND	Ground
26	GND	Ground
27	VCC	Power supply input
28	VDC	High-voltage DC bus input
29	VDC	High-voltage DC bus input
30	BU	U-phase floating supply (referenced to U phase node)
31	U	U-phase output
32	SU	U-phase ground return
33	BV	V-phase floating supply (referenced to V phase node)
34	V	V-phase output
35	SV	V-phase ground return
36	BW	W-phase floating supply (referenced to W phase node)
37	W	W-phase output
38	SW	W-phase ground return

ABSOLUTE MAXIMUM RATING[1)]

PAx/PBx General Purpose I/O Pins Voltage .....-0.3V to 5.8V
LDO Input Voltage V_{CC1} ..... -0.3V to 35V
LDO Output Voltage V_{5V} ..... -0.3V to 6V
LDO Output Current I_{5V} ..... -0.3mA to 100mA
VDC Input Voltage V_{DC}..... -0.3V to 600V
High-Side Floating Supply VB ..... -0.3V to 600V
High-Side Floating Return VS ..... VB-20V to VB+0.3V
Gate Driver Supply Voltage V_{CC2} ..... -0.3V to 22V
Gate Driver Input Voltage V_{IN} .....-0.3V to VCC2+0.3V
Total Current Flowing to VDD SUMIVDD 120mA
Total Current Flowing to VSS SUMIVSS ..... -120mA
Maximum Current per VSS Pin IVSS(pin) ..... -100mA
Pin Injection Current I_{INJ} ..... -10 to 20mA
Total Injection Current $SUMI_{INJ}$ ..... -50 to 50mA
Environmental Temperature T_A ..... -40C to 125℃
Storage Temperature T_{STG} ..... -55C to 150℃
Operating Junction Temperature T_J .....150℃
Electrostatic Protection ESD(HBM) ..... ±2kV

RECOMMENDED OPERATING CONDITIONS

Input Voltage V_{IN} .....4.5V to 60V
Output Voltage V_{OUT}.....0.8V to Dmax x V_{IN} V
Operating Junction Temperature .....-40ºC to 125℃
LDO Input Voltage V_{CC1} ..... 7V to 35V
VDC Input Voltage V_{DC} ..... 0V to 500V
Gate Driver Supply Voltage V_{CC2} ..... 10V to 20V
High-Side Floating Supply VB-VS ..... 10V to 20V
High-Side Floating Return VS ..... 0V to 500V
Operating Voltage VDDH ..... 2.0V to 5.5V
Analog Operating Voltage VDDA ..... 2.0V to 5.5V
I/O Input Voltage V_{IN} ..... -0.3V to 5.5V
CPU Frequency f_{CPU} 108MHz
AHB Clock Frequency f_{AHB} 108MHz
APB Clock Frequency f_{APB} 48MHz
Environmental Temperature (TA) ..... -40C to 125℃
THERMAL PERFORMANCE RthJA RthJC SSOP38..... TBD ℃/W

Notes:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.

2) The JWP79336DM67 includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.

3) The device is not guaranteed to function outside of its operating conditions.

ELECTRICAL CHARACTERISTICS

LDO conditions: V_{IN}=10V, I_{OUT}=40mA, C_{IN}=0.33uF, C_{OUT}=0.1uF, T_A=25ºC, unless otherwise noted. Pre-driver static parameters: V_{CC2}=V_B=15V, V_S=V_{SS}=0V, C_L=0pF, T_A=25ºC Pre-driver dynamic parameters: CL=500pF unless otherwise noted.

Advance information, not production data, subject to change without notice.

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
LDO Electrical Characteristics						
LDO Input Voltage (Operating)	VCC1	-	7	-	35	V
LDO Output Voltage	VOUT		4.8	5.0	5.2	V
LDO Output Voltage	VOUT	1mA<=IO<=40mA, PD<=15W	4.5	-	5.4	V
Line Regulation	Regline	7V<=VIN<=20V	-	10	75	mV
Line Regulation	Regline	8V<=VIN<=20V	-	8	54	mV
Load Regulation	Regload	1mA<=IO<=100mA	-	5	60	mV
Load Regulation	Regload	1mA<=IO<=40mA	-	5	30	mV
Quiescent Current	IQ		-	4	6	mA
Quiescent Current Change	dIQ	1mA<=IO<=40mA	-	0.5	-	mA
Quiescent Current Change	dIQ	8V<=VIN<=20V	-	1	-	mA
Ripple Rejection	RR	6.3V<=VIN<=16.3V, f=120Hz	41	49	-	dB
Short-Circuit Current Limit	ISC	VIN=35V	-	50	-	mA
Dropout Voltage	VIN-VOUT	dVOUT=1%, IOUT=40mA	-	1	-	V
Peak Output Current	IPK		-	150	-	mA
Continuous Output Current Capability	IOUT	With proper thermal design	-	-	100	mA
Gate Driver Electrical Characteristics						
VCC UVLO Positive Threshold	VUVCC+	-	8.0	8.9	9.4	V
VCC UVLO Negative Threshold	VUVCC-	-	7.2	8.2	8.8	V
VBS Quiescent Current	IQBS	-	-	50	100	uA
VCC Quiescent Current	IQCC	-	-	300	450	uA
Thermal Shutdown Temperature	TSD+	-	-	150	-	C
Recovery Temperature after TSD	TSD-	-	-	135	-	C
Turn-on Propagation Delay	tONH	CL=500pF	350	470	600	ns
Turn-off Propagation Delay	tOFFH	CL=500pF	350	470	600	ns
Built-in Dead Time	DT	CL=500pF	700	860	1000	ns
Delay Matching (tON/tOFF)	MT	-	-	-	50	ns

Output Rise Time	tR	CL=500pF	-	730	-	ns
Output Fall Time	tF	CL=500pF	-	80	-	ns
MOSFET Electrical Characteristics						
Drain-Source Breakdown Voltage	VDSS	ID=250uA, VGS=0V	600	-	-	V
Continuous Drain Current	ID	TC=25℃	-	-	4.0	A
Static On-Resistance	RDS(on)	VGS=10V, ID=2.0A	-	2.0	2.4	Ohm
Drain-Source Leakage Current	IDSS	VDS=600V, VGS=0V	-	-	1	uA
Body-Diode Forward Voltage	VSD	VGS=0V, IS=2.0A	-	1.4	-	V
Reverse Recovery Time	trr	VGS=0V, IS=4A, diF/dt=100A/us	-	70	-	ns

Notes:

1) Guaranteed by design.

ELECTRICAL CHARACTERISTICS (CONTROL CORE)

System Reset and Voltage Monitor

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Band gap voltage	V_{BG}	-	-	1.2	-	V
Low power band gap Voltage	V_{LPBG}	-	-	1.1	-	V
Power on reset voltage	V_{POR}	0V up to VDDA, TA= -40~125°C	1.6	1.8	2.1	V
Power off reset voltage	V_{PDR}	Down to 0V, TA= -40~125°C	1.5	1.6	1.75	V
Reset delay time	t_{RSTPOR}	Power on reset	-	3	-	ms
	t_{RSTN}	External reset	-	5	-	us
Low voltage reset	V_{LVR}	LVRS=000	-	1.6	-	V
		LVRS=001	-	1.8	-	
		LVRS=010	-	2.0	-	
		LVRS =011	-	2.5	-	
		LVRS=100	-	2.8	-	
		LVRS=101	-	3.0	-	
		LVRS=110	-	3.5	-	
		LVRS=111	-	4.0	-	
LVR release hysteresis	$V_{HYS(LVR)}$	VDDA = 3.3V, TA = 30°C	-	0.1	-	V
LVR working current	I_{LVR}	VDDA = 3.3V, TA = 30°C	-	6	-	uA
LVD detection voltage	V_{LVD}	LVLS= 000	-	2.0	-	V
		LVLS = 001	-	2.2	-	
		LVLS = 010	-	2.4	-	
		LVLS = 011	-	2.7	-	
		LVLS = 100	-	2.9	-	
		LVLS = 101	-	3.1	-	
		LVLS = 110	-	3.6	-	
		LVLS = 111	-	4.5	-	
LVD release hysteresis	$V_{HYS(LVD)}$	VDDA = 3.3V, TA = 30°C	-	0.1	-	V
LVD working current	I_{LVD}	VDDA = 3.3V, TA = 30°C	-	6	-	uA

Internal Reference Voltage

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Internal reference voltage	V_{REFINT}	T_A= -40~125°C, VFS=0	-	1.6	-	V
		T_A= -40~125°C, VFS=1	-	2.45	-	V
Distribution of the internal reference voltage within the temperature range	ΔV_{REFINT}	VDDA=3.3V, T=-40~125°C	-5	0	1	mV
Temperature coefficient	T_{coeff}	VDDA = 3.3V, TA = 30°C	-	50	-	ppm/℃

Current Characteristics

The typical operating voltage of the device is 3.3V/5.0V. Here the values are tested with VDD=3.3V (TA = 25□) unless stated specifically.

Parameter	Symbol	Peripheral status	Conditions	Min.	Typ. 3.3V	Typ. 5V	Max.	Unit
Operating current	I_{RUN}	Turn off	MCLK=8MHz, RCH/2	-	2.2	2.3	-	mA
			MCLK=16MHz, RCH	-	3.9	4.0	-	
			MCLK=24MHz, RCH+PLL ON	-	4.4	4.9	-	
			MCLK=48MHz, RCH+PLL ON	-	7.5	8.2	-	
			MCLK=72MHz, RCH+PLL ON	-	8.2	8.7	-	
			MCLK=96MHz, RCH+PLL ON	-	9.9	10.3	-	
			MCLK=108MHz, RCH+PLL ON	-	10.5	11.0	-	
		All turn on, ADC sampling turns on	MCLK=8MHz, RCH/2	-	5.8	6.6	-	
			MCLK=16MHz, RCH	-	7.7	8.5	-	
			MCLK=24MHz, RCH+PLL ON	-	8.2	9.3	-	
			MCLK=48MHz, RCH+PLL ON	-	8.4	9.7	-	

The typical operating voltage of the device is 3.3V/5.0V. Here the values are tested with VDD=3.3V (TA = 25℃) unless stated specifically.

Parameter	Symbol	Peripheral status	Conditions	Min.	Typ. 3.3V	Typ. 5V	Max.	Unit
			MCLK=72MHz, RCH+PLL ON	-	11.3	12.6	-	
			MCLK=96MHz, RCH+PLL ON	-	13.0	14.3	-	
			MCLK=108MHz, RCH+PLL ON	-	15.2	16.3	-	
Sleeping current	I_{SLEEP}	Turn off	MCLK=8MHz, RCH/2	-	0.5	0.6	-	mA
			MCLK=16MHz, RCH	-	0.6	0.7	-	
			MCLK=24MHz, RCH+PLL ON	-	1.3	1.8	-	
			MCLK=48MHz, RCH+PLL ON	-	2.2	2.7	-	
			MCLK=72MHz, RCH+PLL ON	-	3.4	4.0	-	
			MCLK=96MHz, RCH+PLL ON	-	3.6	4.1	-	
			MCLK=108MHz, RCH+PLL ON	-	4.0	4.5	-	
		All turn on, ADC sampling turns on	MCLK=8MHz, RCH/2	-	3.8	4.5	-	
			MCLK=16MHz, RCH	-	4.5	4.9	-	
			MCLK=24MHz, RCH+PLL ON	-	5.6	6.5	-	
			MCLK=48MHz, RCH+PLL ON	-	7.5	8.7	-	
			MCLK=72MHz, RCH+PLL ON	-	10.5	11.5	-	
			MCLK=96MHz, RCH+PLL ON	-	12.0	12.7	-	
			MCLK=108MHz, RCH+PLL ON	-	13.0	13.6	-	

Notes:

The following conditions apply to the measurement of current characteristics:

* All IOs are set to output low and no load.
* All modules have no load only with clock on unless specifically stated.

Current Consumption in Stop/ULP Stop Modes

Parameter	Symbol	Conditions	Supply voltage	LDO Drive mode set to 50uA	Unit
Stop current (turn off all high frequency clocks and PLL)	I_{STOP}	All modules shut down	3.3V	55	uA
			5V	57	
		Only LVR and LVD turn on	3.3V	60	
			5V	63	
		Only WT turns on	3.3V	55	
			5V	58	
ULP Stop Current (turn off all high frequency clocks and PLL, change to low power LDO)	$I_{ULTSTOP}$	All modules shut down	3.3V	7.0	uA
			5V	8.0	
		Only WT turns on	3.3V	7.1	
			5V	8.1	

Wake-up from Low Power Modes

Parameter	Symbol	Min.	Typ.	Max.	Unit
Wake-up time from Stop mode	t_{STOP}	-	100	-	us
Wake-up time from ULP Stop mode	$t_{ULTSTOP}$	-	240	-	

External Clock Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
OSCL frequency	f_{OSCL_ext}	-	32.768	-	kHz
OSCL_IN input high voltage	V_{OSCLH}	-	0.5	-	V
OSCL_IN input low voltage	V_{OSCLL}	-	0	-	

External Oscillator Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
OSCL current	I_{OSCL}	VDDH=3.3V, GAIN=00	-	0.70	-	uA
		VDDH=3.3V, GAIN=01	-	0.85	-	
		VDDH=3.3V, GAIN=10	-	1.25	-	
		VDDH=3.3V, GAIN=11	-	1.35	-	
OSCL set up time	$t_{SU(OSCL)}$	GAIN=00	-	0.25	-	s
		GAIN=01	-	0.15	-	
		GAIN=10	-	0.11	-	
		GAIN=11	-	0.15	-	

Internal Clock Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
RCH frequency	F_{RCH}	After calibration	-	16	-	MHz
RCH TRIM	$TRIM_{RCH}$	VDDH = 3.3V, TA = 30°C	-	2	-	%
RCH duty cycle	$DuCy_{RCH}$	-	-	50	-	%
RCH accuracy	ACC_{RCH}	-	-	1	2.4	%
RCH set up time	$t_{SU(RCH)}$	-	-	6	-	us
RCH operating current	I_{RCH}	-	-	130	-	uA
RCL frequency	F_{RCL}	-	-	32	-	kHz
RCL TRIM	$TRIM_{RCL}$	VDDH = 3.3V, TA = 30°C	-	0.8	-	%
RCL set up time	$DuCy_{RCL}$	-	-	50	-	%
RCL accuracy	ACC_{RCL}	-	-	-	10	%
RCL set up time	$t_{SU(RCL)}$	VDDH = 3.3V, TA = 30°C	-	125	-	us
RCL operating current	I_{RCL}	VDDH = 3.3V, TA = 30°C	-	300	-	nA

PLL Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
PLL input frequency	f_{PLL_IN}	4	16	30	MHz
PLL input duty cycle	$DuCy_{PLL}$	30	50	70	%
PLL output frequency	f_{PLL_OUT}	30	108	256	MHz
PLL lock time	t_{LOCK}	-	5	14	us
PLL jitter	$Jitter_{PLL}$	-	13	40	ps

Flash Storage Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Byte programming time	t_{prog}	-	-	-	8.5	us
Page erase time	t_{ERASE}	-	2	-	3	ms
Total erase time	t_{ME}	-	30	-	40	ms
Programming current	I_{prog}	-	-	0.5	0.8	mA
Erasing current	I_{ERASE}	-	-	-	0.8	mA
Endurance	N_{END}	-	100000	-	-	Cycles
Retention time	t_{RET}	TA = 25°C	100	-	-	Years
		TA = 85°C	20	-	-	

ESD Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
HBM	V_{HBM}	MIL-STD-883H	±4000	-	-	V
CDM	V_{CDM}	JESD22-C101E	±1000	-	-	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Latch-up trigger current	I_{LAT}	JEDEC standard NO.78D 2011.11	±200	-	-	mA
VDDH/VDDA over voltage	V_{LAT}		6.5	-	-	V

I/O Characteristics

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
IO input high voltage	V_{IH}	VDDH = 5V		-	2.0	-	V
		VDDH = 3.3V		-	1.5	-	
IO input low voltage	V_{IL}	VDDH = 5V		-	1.2	-	
		VDDH = 3.3V		-	1.0	-	
Input hysteresis	V_{HYS}	VDDH = 5V		-	0.5	-	V
		VDDH = 3.3V		-	0.4	-	
Output source current	I_{OH}	VDDH=3.3V VOH=0.7*VDDH	Weak drive (DR=1)	-	20	-	mA
			Strong drive (DR=0)	-	40	-	
		VDDH=5V VOH=0.7*VDDH	Weak drive (DR=1)	-	40	-	
			Strong drive (DR=0)	-	80	-	
Output sink current	I_{OL}	VDDH=3.3V VOL=0.4V	Weak drive (DR=1)	-	10	-	mA
			Strong drive (DR=0)	-	20	-	
		VDDH=5V VOL=0.6V	Weak drive (DR=1)	-	20	-	
			Strong drive (DR=0)	-	45	-	
IO input high current	I_{IH}	VDDH = 5V		-	-	0.1	uA
		VDDH = 3.3V					
IO input low current	I_{IL}	VDDH = 5V		-0.1	-	-	uA
		VDDH = 3.3V					
IO output high voltage	V_{OH}	VDDH = 5V	Strong drive I_{min}=16mA Weak drive I_{min}=8mA	4.5	-	-	V

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
		VDDH = 3.3V	Strong drive I_{min}=16mA Weak drive I_{min}=8mA	2.5	-	-	V
IO output low voltage	V_{OL}	VDDH = 5V	Strong drive I_{min}=16mA Weak drive I_{min}=8mA	-	-	0.3	V
		VDDH =3.3V	Strong drive I_{min}=16mA Weak drive I_{min}=8mA	-	-	0.4	V
Total output current	I_{total}	All ports		-	100	-	mA
Pull-up resistor	R_{pu}	V_{IN}=NULL		-	55	-	k
Pull-down resistor	R_{pd}	V_{IN}=NULL		-	55	-	
Filter width	$T_{PW(IO)}$	External Reset pin		-	4	-	us
I/O capacitance	C_{IO}	-		-	-	10	pF

ADC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{adc}	Vref+=4.9V(VFS=1)	4	-	5.5	V
		Vref+=3.2V(VFS=0)	2.2	-	5.5	
Reference voltage	V_{ref+}	-	2	-	VDDA	V
Operating current	I_{ADC}	2MSPS (32MHz)1	-	3.5	-	mA
Operating frequency	f_{ADC}	-	0.1	-	32	MHz
Sampling rate	F_s	VDDA>4V	-	-	2	MSPS
		2.7V<VDDA<4V	-	-	1.5	
		2.2V<VDDA<2.7V	-	0.15	-	
Analog input voltage	V_{AIN}	VFS=1	0	-	4.9 or VDDA	V
		VFS=0	0	-	3.2 or VDDA	
Sampling switching resistor	R_{ADC}	-	-	1	-	k
Internal sampling capacitor	C_{ADC}	-	-	1.2	-	pF
Latency of data preparation	$W_{LATENCY}$	-	-	2.5	-	1/fpclk
Latency of trigger sampling	t_{latr}	-	-	2.5	-	1/fADC

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Sampling time	t_{samp}	-	1	-	16	1/fADC
Conversion time	t_{conv}	-	13	-	16	1/fADC
Start-up time	t_{STAB}	-	32	-	512	1/fADC

Notes：

The maximum operating frequency is 32MHz, and the corresponding sampling frequency can be up-to 2MSPS.

VTS Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Linearity of VSENSE with temperature	T_L	-	±4	-	°C
Average slope of temperature sensitivity Accuracy	A_{vg_slope}	-	4.1	-	mV/°C
Sampling time of ADC getting temperature	t_{S_temp}	-	1	-	us
Voltage at 30°C(±5°C)	V_{30}	-	1.35	-	V

ADC Accuracy

Parameter	Symbol	Conditions	Typ.	Max.	Unit
Unadjusted total error	ET	-	+/-10	+/-40	LSB
Unadjusted offset error	EO	-	+/-5	+/-20	
Unadjusted gain error	EG	-	+/-5	+/-20	
Trim step size	-	-	0.8	-	
Trim range	-	-	-	+/-100	
Differential linearity error	ED	-	1	2	
Integral linearity error	EL	-	1	4	

OPA Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{OPA}	-	1.8	3.3	5.5	V
Common mode input range	CMIR	-	0	-	VDDA	V
Input offset voltage	VI_{OFFSET}	No calibration, TA = -40~125°C	-2.0	0	3.0	mV
		After calibration, TA = -40~125°C	0.15	-	0.25	mV
Input offset voltage drift	ΔVI_{OFFSET}	-	-	0.05	-	uV/°C
Drive current	I_{LOAD}	-	-	5	-	mA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Dray current	I_{DD}	No load capacitance	-	80	-	uA
Common mode rejection ratio	CMRR	VDDA=3.3V, T_A = 30°C, C_L = 30pF	-	145	-	dB
Power supply rejection ratio	PSRR	VDDA=3.3V, T_A = 30°C, C_L = 30pF	-	130	-	dB
Bandwidth	GBW	VDDA=3.3V, T_A=30°C, offset current=4uA	-	10	-	MHz
Slew rate	SR	VDDA =5V, T_A = 30°C, C_L = 30pF	-	3.5	6	V/us
Resistive load	R_{LOAD}	-	0.1	10	-	k
Capacitive load	C_{LOAD}	-	-	100	-	pF
High saturation voltage	VOH_{SAT}	-	-	3.8	-	mV
Low saturation voltage	VOL_{SAT}	-	-	3.3	-	mV
Phase margin	φm	VDDA=3.3V, T_A=30°C, C_L=50pF, offset current=4uA	-	25	-	°

ACMP Characteristics

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage		V_{ACMP}	-	1.8	3.3	5	V
Input offset voltage		V_{os}	-	-	-	13	mV
Input common mode voltage		V_{cm}	Response time <160ns	0	-	VDDA	V
Compare hysteresis		V_{hyster}	-	-	20	-	mV
Transfer delay		T_{str}	CPDLY = 00, VDDA = 5V, FREN=0	-	40	-	ns
			CPDLY = 00, VDDA = 3.6V, FREN=0	-	50	-	
			CPDLY = 00, VDDA = 2.5V, FREN=0	-	60	-	
			CPDLY = 01, VDDA = 5V, FREN=0	-	120	-	
			CPDLY = 01, VDDA = 3.6V, FREN=0	-	145	-	
			CPDLY = 01, VDDA = 2.5V, FREN=0	-	200	-	
			CPDLY = 10, VDDA = 5V, FREN=0	-	320	-	
			CPDLY = 10, VDDA = 3.6V, FREN=0	-	450	-	ns
			CPDLY =10, VDDA = 2.5V, FREN=0	-	550	-	
			CPDLY = 11, VDDA = 5V, FREN=0	-	750	-	
			CPDLY = 11, VDDA = 3.6V, FREN=0	-	1000	-	
			CPDLY = 11, VDDA = 2.5V, FREN=0	-	1200	-	
Respon se time	Rising edge	T_{rt}	Normal response	-	50	-	ns

Parameter		Symbol	Conditions	Min.	Typ.	Max.	Unit
	Falling edge			-	55	-	
	Rising edge		Quick response	-	30	-	
	Falling edge			-	40	-	
Operating current		I_{cmp}	VDDA=5V, one channel of ACMP working	-	12	-	uA
Error offset ratio		dV_{offset}/dT	-	-	0.5	-	μV/°C

DAC Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V_{DAC}	-	1.8	3.3	5	V
Conversion time	t_{conv}	1LSB output variation, CL=1pF	-	280	-	ns
Settling time	t_{settle}	VDDA = 3.3V, from 0V output to maximum full amplitude value, CL=1pF	-	0.8	-	us
Output voltage	V_{OUT}	-	0.001	-	5.0	V
Operating current	I_{DAC}	-	-	200	-	uA
Resistive load	R_{load}	-	-	-	1	kΩ
Capacitive load	C_{load}	-	-	-	10	pF
Integral non-linearity error	I_{NL}	-	-	0.9	-	LSB
Differential non-linearity error	D_{NL}	-	-	0.75	-	LSB
Offset error	Offset	-	-	1.5	-	mV
Gain error	Gain error	-	-	0.4	-	%
Time of WAKEUP	t_{WAKEUP}	-	-	5	-	us
Power supply rejection ratio	PSRR	Min. 1KHz, max. 1MHz	90	-	100	dB

FUNCTIONAL DESCRIPTION

Temperature output

The VTS Pin is the output of the temperature detection. The relationship between the output voltage and temperature is shown in the following curve.

TBD

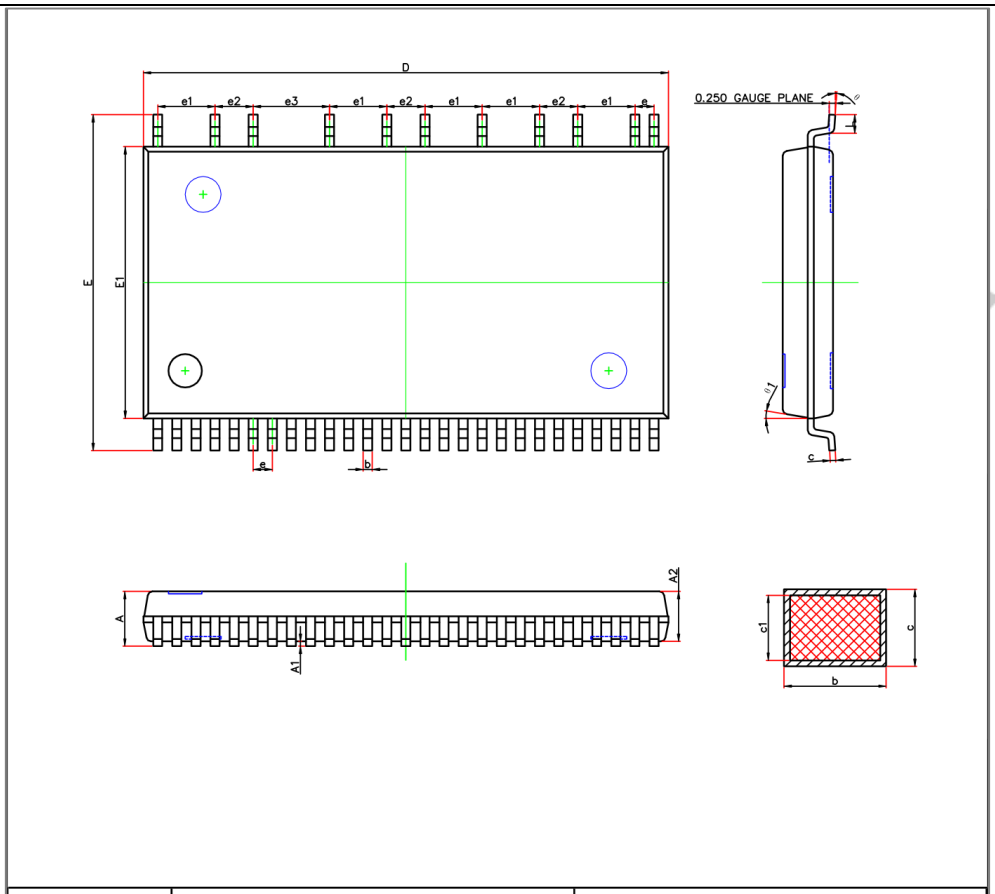
REFERENCE DESIGN

Note: Information in the following reference design sections is not part of JoulWatt component specification. Customers are responsible for determining suitability of components chosen for their purposes and should validate their design implementation to make sure the proper system functionality.

TBD

PACKAGE OUTLINE

SSOPA54-38 UNIT:



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	-	2.350	-	0.093
A1	0.000	0.200	0.000	0.008
A2	2.000	2.200	0.079	0.087
b	0.370	0.390	0.012	0.020
c	0.236	0.320	0.009	0.013
D	21.800	22.200	0.858	0.874
e	0.80(BSC)		0.031(BSC)	
e1	2.40(BSC)		0.094(BSC)	
e2	1.60(BSC)		0.063(BSC)	
e3	3.20(BSC)		0.126(BSC)	
E	13.800	14.400	0.543	0.567
E1	11.200	11.600	0.441	0.457
L	0.600	1.000	0.024	0.039
θ	0°	10°	0°	10°
θ1	10°	12°	10°	12°

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REVISION HISTORY

REV	DATE	DESCRIPTION	NAME
Rev.0.1	05/13/2026	Initial revision	